

REMARKS

The Examiner's Office Action mailed on May 16, 2005 has been received and its contents carefully considered.

Claims 1-8 are pending in this application. Claim 2 is canceled without prejudice or waiver, and claim 1 is amended herein. Claims 1, 4 and 5 remain the independent claims in this application.

In the current Action, claims 1-3 and 5-8 are rejected under 35 U.S.C. §102(b) as being anticipated by Murata et al. (U.S. Patent No. 4,759,010). Claim 1 is amended herein to further distinguish the invention over the applied reference.

Anticipation under 35 U.S.C. §102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Although anticipation requires only that the claim under attack "read on" something disclosed in the reference, all limitations of the claim must be found in the reference, or "fully met" by it.

As amended herein, claim 1 includes the further limitation "wherein with respect to the read-out controlling means, the first memory means and the second memory means are each independently capable of simultaneously writing and reading (emphasis added). The present application, with regard the exemplary embodiment shown in Figure 2, discloses at page 11, lines 16-18 (Amended Specification), that the speech control memories 26a, 26b are independent two-port memories, capable of writing and reading simultaneously. However, the memories 12 and 13, shown in Figure 7 of Murata, are one-port memories that cannot be written and read independently at the same time. As Murata discloses, circuit 114 inverts the write enable signal WE2, which has been supplied to the second memory 13, to give a read enable (column 6, a line 67 through column 7, line 1). This shows that one signal is used to enable both writing and reading, with the result that one of the memories is in the write mode while the other is in the read mode. Therefore, the memories 12 and 13 in Murata cannot be written and read independently at the same time.

For at least the foregoing reason, it is respectfully submitted that claim 1, as well as claims 3 and 5-8, patentable distinguish over the applied prior art.

Claim 4 stands rejected under 35 U.S.C. §103(a) as being obvious over Murata per et al. in view of Kawai (U.S. Patent No. 4,972,407). The rejection is respectfully traversed.

With respect to claim 4, the Examiner asserts that Murata discloses the recited multiplexing means, switching control means, including a switching correspondence means, and demultiplexing means, where the switching correspondence means comprises an information receiving means, a network switching control means and a read-out controlling means. However, the Examiner expressly acknowledges that Murata fails to teach two other recited features of the switching correspondence means, namely, "working memory means for storing the connection information from the information receiving means, the working memory means reading out as a read-out signal the stored connection information in response to the switching signal from the network switching control means; and read-out selection means for selecting the connection information from one of the working memory means and the information receiving means, and outputting the selected connection information in response to the switching signal from the network switching control means."

To cure these deficiencies in Murata, the Examiner points to Figure 4 of Kawai as teaching working memory means 43 for storing the connection information from the information receiving means 44, the working memory means reading out as a read-out signal the stored connection information in response to the switching signal from the network switching control means; and read-out selection means 42 for selecting the connection information from one of the working memory means 43 and the information receiving means 44, and outputting the selected connection information in response to the switching signal from the network switching control means. The Examiner argues it would have been obvious to one skilled in the art to modify Murata to have a selector to choose between the working memory and the information receiving means as taught by Kawai in order to reduce hardware size (column 2, lines 18-19).

The Applicants respectfully disagree. Kawai discloses that in Figure 4, reference numeral 41 denotes a data buffer memory ("DM"), 42 denotes a selector ("SEL"), 43 denotes an address controlled memory ("ACM"), 44 denotes a counter, and 45 denotes an exchange control circuit (column 3, line 66 through column 4, line 2). All time slots

in one cycle of input data, which is time-division multiplexed data, are successively written into data buffer memory 41 according to successive addresses supply from the counter 44 (column 5, lines 3-7). On the other hand, the exchange control circuit 45, in advance, sets the contents of the address control memory 43 so that the required exchanges of time slots are achieved when the time-division multiplexed data is read out of data buffer memory 41 on the next cycle (column 3, lines 31-38). In other words, the function of selector 42 is to select either a uniform sequence of increasing addresses from counter 44, or a sequence of addresses for exchanging time slots stored in address control memory 43, depending upon whether the data buffer memory 41 is in a write mode or in a read mode. The function of counter 44 is simply to generate successive addresses, and accordingly, it does not, as the Examiner asserts, correspond to the "information receiving means" recited in claim 1. Rather, it appears that that function is performed by the exchange control circuit 45. However, the exchange control circuit 45 only provides exchange control data to the address control memory 43, and not to selector 42. Thus, it is submitted that, contrary to the Examiner's position, the circuit in Figure 4 of Kawai fails to teach or suggest a "read-out selection means for selecting the connection information from one of the working memory means and the information receiving means."

As already noted, the Examiner asserts with regard to claim 4 that the base reference, Murata, discloses a "read-out controlling means for storing the connection information (control data D), and for sequentially reading out the stored connection information in read-out order of the switching memory means 20 (Column 6 Line 34-37)". The text referenced by the Examiner discusses first memory 12, which is shown in Figure 7 as receiving control data from data register 112, while claim 1 requires that the read-out controlling means store the connection data "outputted by the readout selection means." It is not understood from the Examiner's argument how the circuit elements of Kawai, such as the "readout selection means" are to be combined with those of Murata to achieve the circuit configuration recited in claim 4. Moreover, it would appear that the combination suggested by the Examiner would make second memory 13 and other elements redundant. Accordingly, the Applicants believe that in this case, the Examiner has impermissibly picked and chosen from the references only as much as support a

given position, to the exclusion of other parts necessary to the full appreciation of what such references fairly suggest to one of ordinary skill in the art.

What the Kawai referenced fairly suggests may be gleaned from column 5, lines 22-29, which state that "[i]n practice, the time division switching circuit in the embodiment of the present invention has a double buffer construction, i.e., has the construction of Fig. 4 doubly, and uses one side of the double construction for writing into data buffer memory 41 and the address control memory 43, and the other side for reading out the data buffer 41, alternatively for each cycle of the input." It is submitted this suggests to one of ordinary skill in the art the invention of Murata, rather than the present invention.

New claims 9 and 10 are added to cover additional features disclosed in the present application.

In summary, it is submitted that this Amendment places the application in condition for allowance. Notice of such and the passing of this application to issuance are earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange such an interview.

Respectfully submitted,

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Date



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